REMARKS

Below, the applicant's comments are preceded by related remarks of the examiner set forth in small bold type.

Claims 1-6 and 8-28 are rejected under 35 U.S.C. 103(a) as being unpatentable over Glew et al. (5,561,780) in view of "The Cache Memory Book" by Jim Handy.

Regarding Claims 1-6 and 10, Glew et al. teaches a buffer 132 ("cache") with a number of cache-line sized storage locations 136 ("cache lines") and an eviction unit 139 enabled to evict data from the storage locations when partial writes fill a single storage location one storage portion 140 ("cache line has multiple portions") at a time. A thirty-two-byte validity filed 144 ("validity bit storage") monitors which of the thirty-two portions of the storage locations have been written to. When the thirty-two-byte validity field 144 determines that all the thirty-two portions of the storage locations are till, the storage location ("cache line") is evicted (See Figure 4 and Column 4, lines 59-67 and Column 7, lines 1-30). Glew et al. also discloses that storage in the buffer 132 is very much like storage on an on-chip cache unit (DCU), therefore, as a DCU, buffer 132 may store data corresponding to locations in main memory (See Column 1, lines 25-38 and Column 7, lines 30-32). Glew et al. does not teach buffer 132 being part of a coherency protocol. Handy teaches cache coherency which prevents stale data from being confused with current data (page 124). It would have been obvious to one of ordinary skill in the art at the time the invention was made to integrate the cache coherency of Handy to the buffer of Glew et al. and integrating a cache coherency protocol such as that of Handy. A coherency protocol would prevent the confusion between good and useless data. In integrating a cache coherency protocol to the invention of Glew et al., small delays in between data evictions must be added; however, adding the delay of a cache coherency protocol would prevent the delays caused by accessing stale data in the cache. Additionally, although Glew et al. discloses that "processor ordering is ignored", this does not mean that a coherency protocol cannot be implemented since in the case of Glew et al. a coherency protocol and processor ordering are two separate concepts. In adding a coherency protocol in the system of Glew et al. the protocol can ensure coherency between multiple microprocessors A through D (see Figure 3) and thus, processor ordering is not necessary.

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Regarding Claims 13, 15, 18, 22-26 and 28, Glew et al. teaches a buffer 132 ("cache") with a number of cache-line sized storage locations 136 ("cache lines") being written to through the use of a write combining unit 138, and an eviction unit 139 enabled to evict data from the storage locations when partial writes fill a single storage location one storage portion 140 ("cache line has multiple portions") at a time.

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The system of Glew et al. initiates write transactions through an execution device 126 (Figure 3).

The applicant respectfully disagrees. Claim 1 requires "cache lines to store data, at least a portion of the data to be written to a main memory." While Glew discloses a write-combining buffer in which "[s]torage into the buffer lines is accomplished in much the same manner that a DCU employs for storing data within cache-lines," (col. 7:30-33), the write-combining buffer stores uncacheable data (col. 10:38-40), which are not written to a main memory. Glew teaches storing a value to "indicate whether data is cacheable or uncacheable, with only uncacheable data write operations being processed using the write-combining buffer" (col. 10:33-40). An example of uncacheable data is graphics data, which are sent to a display device to control the display of pixels (col. 2:32-39). Glew does not disclose or suggest that the write-combining buffer stores data, and "at least a portion of the data to be written to a main memory."

Moreover, Glew does not disclose or suggest "an eviction mechanism to evict data stored in one of the cache lines based on validity state information associated with the data stored in the cache line, the eviction mechanism to send the evicted data to the main memory," as recited in claim 1. In Glew, the data evicted from the write-combining buffer 132 are not sent to a main memory, but are, for example, sent to a display device.

What is lacking in Glew is also not disclosed or suggested in Handy, which discloses a MESI protocol.

Claims 10 and 13 are patentable for at least the same reasons as claim 1.

Claims 18 and 22 would not have been obvious in view of Glew and Handy. The examiner acknowledges that Glew's system initiates write transactions through an execution device 126 (FIG. 3). As Glew's execution device 126 resides in a microprocessor 110, the execution device is clearly not an input/output device. Examples of input/output devices include "a keyboard, a mouse, a sound card, a video card, a digital scanner, a digital camera, a network card, a modem" (see page 11, lines 2-24 of the application). The applicant respectfully requests the examiner to

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indicate which passages in Glew would have made obvious the portions of the applicant's claims that recite: "a cache memory to store write data sent from an input/output device," (claim 18), or "initiating write transactions by an input/output device to write data [and] writing the data into a cache memory" (claim 22).
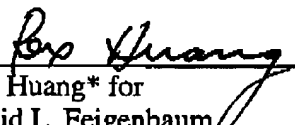
The dependent claims are patentable for at least the same reasons as the claims on which they depend.

Any circumstance in which the applicant has (a) addressed certain comments of the examiner does not mean that the applicant concedes other comments of the examiner, (b) made arguments for the patentability of some claims does not mean that there are not other good reasons for patentability of those claims and other claims, or (c) amended a claim does not mean that the applicant concedes any of the examiner's positions with respect to that claim or other claims.

Please apply $950 for the three-month extension fee, and $90 for the excess claims fee, and any other charges, to deposit account 06-1050, referencing attorney docket 10559-639001.

Respectfully submitted,

Date: _8/11/2004_

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* See attached document certifying that Rex Huang has limited recognition to practice before the U.S. Patent and Trademark Office under 37 CFR § 10.9(b).

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Expires: January 1, 2005

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